**UNIVERSITY OF ENGINEERING AND TECHNOLOGY  
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**AMBA AHB-Lite Protocol Verification Plan**

Submitted By:

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**AHB-Lite Protocol:**

**Working of Protocol:**

**Global Signals:**

|  |  |  |
| --- | --- | --- |
| **Name** | **Destination** | **Description** |
| HCLK | Clock source | Clock source for all operations on the protocol. Input signals are sampled at rising edge and changes in output signals happen after the rising edge |
| HRESTn | Reset Controller | Asynchronous primary reset for all bus elements |

**Master Signals:**

|  |  |  |
| --- | --- | --- |
| **Name** | **Destination** | **Description** |
| HADDR [31:0] | Slave and Decoder | Address bus of 32 bits |
| HBURST [2:0] | Slave | Indicates the type of burst signal including wrapping and incrementing bursts |
| HSIZE [2:0] | Slave | Indicates the size of transfer from 8 bits to 1024 bits |

**Slave Signals:**

|  |  |  |
| --- | --- | --- |
| **Name** | **Destination** | **Description** |
| HRDATA [31:0] | Multiplexor | Read data bus to transfer the data from a Slave’s location to the Master via multiplexor |
| HREADYOUT | Multiplexor | Indicates transfer has finished on the bus and is used to extend the data phase |
| HRESP | Multiplexor | Provides additional information that the transfer was successful or failed |

**Decoder Signals:**

|  |  |  |
| --- | --- | --- |
| **Name** | **Destination** | **Description** |
| HSELx Note: x is a unique identifier for AHB lite slave | Slave | Indicates current transfer is for intended for selected slave |

**Multiplexor Signals:**

|  |  |  |
| --- | --- | --- |
| **Name** | **Destination** | **Description** |
| HRDATA [31:0] | Master | Read data bus to rout to Master |
| HREADY | Master and Slave | Indicates completion of previous transfer |
| HRESP | Master | Transfer response |

**Software/Tools:**

QuestaSim  
Github  
LaTex

# Verification Plan

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **No.** | **Feature** | **Test Description** | **Ref.** | **Type** | **Result** | **Comments** |
| 1 | Write Transfer from Master to Slave | When HWRITE is high then the Master will broadcast the data on the HWDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping types. | 3.1 | TR |  | Successful write. HRESP should be low and HREADY should be high |
| 2 | Read Transfer from Slave to Master | When HWRITE is low then the slave must generate the data on the HRDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping type. | 3.1 | TR |  | Successful read. HRESP should be low and HREADY should be high |
| 3 | Continuous writing to the same slave at the same address location | When HWRITE is high then the Master will broadcast the data packets on the HWDATA [31:0] bus. | 3.1 | TR |  | Successful write. HRESP should be low and HREADY should be high for the successive data packets |
| 4 | Continuous reading from the same slave and same address location | When HWRITE is low then the slave must generate the data packets on the HRDATA [31:0] bus. | 3.1 | TR |  | Successful read. HRESP should be low and HREADY should be high for the successive data packets |
| 5 | Random Write transfers | When HWRITE is high then the Master will broadcast the data packets on the HWDATA [31:0] bus. | 3.1 | TR |  | Successful write. HRESP should be low and HREADY should be high for the successive data packets |
| 7 | Random Read Transfers | When HWRITE is low then the slave must generate the data packets on the HRDATA [31:0] bus. | 3.1 | TR |  | Successful read. HRESP should be low and HREADY should be high for the successive data packets |
| 8 | Write-Read Transfer | Write transfer followed by Read transfer at a particular address A. | 3.1 | TR |  | HRESP is low, HREADY is high and the address location must have the updated value |
| 9 | Read-Write Transfer | Read transfer followed by Write transfer at a particular address A. | 3.1 | TR |  | HRESP is low, HREADY is high and the slave must return the previous Data (A). |
| 10 | Global Signal: HCLK | A clock signal is generated in the top module | 7.1.1 | A |  | All input signals must be sampled at the rising edge of the clock and changes in the output signals must occur after the rising edge. |
| 11 | Global Signal:  HRESTn | Since this is an active low signal. When asserted then it must reset all bus elements. Note: Slaves must ensure that HREADYOUT is high. HTRANS [1:0] must indicate IDLE. | 7.1.2 | TR |  | All previous binary information in the bust elements will be lost. |
| 12 | Master Signal: IDLE HTRANS [1:0] =b00 | When IDLE transfer is inserted to an address. | 3.2 | TR |  | The HREADY must be low during the IDLE transfer. The transfer must be ignored by the slave. Slave must provide a OKAY response. |
| 13 | Transfer type changed during waited states: Scenario 1 | Transfer type changes from IDLE to NONSEQ during waited states. The HTRANS signal must be kept constant after the transition until HREADY is high | 3.6.1 | A |  | Successfully transfer type changed. Slave must give OKAY response. |
| 14 | Transfer type changed during waited states: Scenario 2 | Transfer type changes from BUSY to SEQ during waited states for fixed length bursts. The HTRANS signal must be kept constant after the transition until HREADY is high | 3.6.1 | A |  | Successfully transfer type changed. Slave must give OKAY response. |
| 15 | Transfer type changed during waited states: Scenario 3 | Transfer type changes from BUSY to any other type during waited states for undefined length burst. The burst continues if a SEQ transfer is performed but terminates if and IDLE or NONSEQ transfer is performed. | 3.6.1 | A |  | Successfully transfer type changed. Slave must give OKAY response. |
| 16 | Transfer type changed during waited states: Scenario 4 | Transfer type changed from IDLE to SEQ. |  |  |  | Slave will give an ERROR response. |
| 17 | Bus Termination |  |  |  |  |  |
| 18 | Slave response:  Transfer done |  |  |  |  |  |
| 19 | Slave response:  Transfer pending |  |  |  |  |  |
| 20 | Slave response:  transfer failed |  |  |  |  |  |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

## Explanation of Different Fields

|  |  |
| --- | --- |
| **No.** | The serial number of the test. |
| **Feature** | The feature which the current test is verifying in full or partially. The feature is usually on the abstraction level of a user. |
| **Test Description** | A detailed description of the test case is performed. You can be as verbose as you want. |
| **Ref.** | Reference to the section in the related standard document. The section number, as well as page numbers, should be described here. |
| **Type** | Type of the test. Whether the test is an assertion (A) or a transaction (T) type. |
| **Result** | Pass (P) or Fail (F). |
| **Comments** | Any other comments about the test or its results that you want to mention. |